



An International Technical Symposium

In association with SENSE-VIT

23rd February 2018- 25th February 2018

VLSI DESIGN WORKSHOP

DESCRIPTION

A two-day workshop on VLSI design by professionals from HT INDIA LABS. Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed.

Over the course of 2 days, participants will be taught various topics including VLSI design methodologies and review of digital systems. Hands-on practical knowledge will be imparted. Participants will be taught design entry methods using Verilog HDL, FSM design and lots of other interesting things. These will surely add feathers to your resume and help you stand out from the crowd.

COURSE STRUCTURE

1.VLSI Design Methodologies

- Classification in Design Approach: Front End/Back End
- Classification in Design implementation : FPGA, CPLD/Semi custom (Standard cell, ASIC)/Full custom (ASIC , AMS)
- VLSI Design Flow & Supporting Tools

2. Overview to physical Design & Implementation

- Post Synthesis simulation Design optimization simulation Floor planning & Clock distribution Placement & Routing (PNR)
- Bit file (Net List) generation & Implementation : FPGA/CPLD/ASIC (Standard cell)

3. Review of Digital System & FSM Design

- Combination & Sequential Logic Circuit
- Sequential Circuits: Counters, Registers, Memory, Sequence Detector. Finite State Machine design Approach
- Sequential Circuit Timing
- Clock skew
- Maximum Clock Frequency Calculation , various Examples
- Design Entry with HDL (VHDL/Verilog)
- HDL Basic: Entry/Module, Structure, Data Objects, Operands.

4. Modelling Techniques:

- Data Flow
- Structural
- Behavioural

5. Design Entry with Verilog HDL & Overview to Programmable Platform

- Design Using Blocking and Non Blocking Statements
- Design Simulation. Design synthesis.
- Modelling Combinational Circuit, Synchronous Logic Circuits, FSM. Introduction to Programmable Platforms (FPGA)
- Basic Components of an FPGA, FPGA Architecture Overview , HDL Coding techniques for efficient FPGA Synthesis , synthesis Techniques and Implementation operations, constraints, Timing Closures, FPGA Design Flow, Static Timing Analysis .

ABOUT HT INDIA LABS

HT INDIA LABS is an initiative towards training students, faculties and professionals in various upcoming and existing technologies. Improving their skills and knowledge, practical and hands on experience on implementation of tools and techniques is provided. They not only give an overview on various tools but believe in educating the participants on practical applications of the same.

They understand the need of practical and industry ready knowledge and keeping this in mind they have put a step forward with different pedagogies. HT INDIA LABS provides a wide range of ongoing job-related education and training to keep students up-to-date on the very latest in technical, job-related and management knowledge.



CERTIFICATION

All the participants will be provided with the certificate from HT INDIA LABS.

DATES OF THE WORKSHOP

23rd & 24th February, 2018

REGISTRATION FEE

Non-IETE member – 900 /participant

IETE member –700 /participant

CONTACT FOR FURTHER DETAILS

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